**A new approach to design fault coverage circuit with efficient hardware utilization for testing applications**

**ABSTRACT**

A new fault coverage test pattern generator using a linear feedback shift register (LFSR) called FC-LFSR can perform fault analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the hardware utilization. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence power consumption is also reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

**LANGUAGE USED:**

* Verilog HDL

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis